Sierra Components, Inc.

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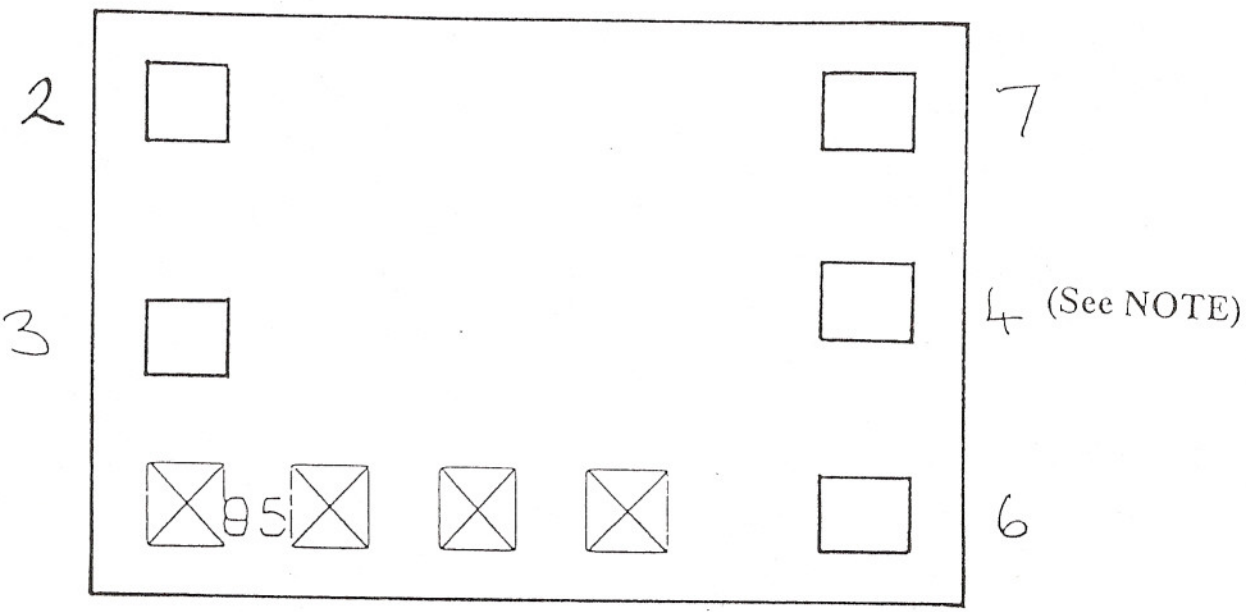
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad	Function
1	NC
2	V_{inv}
3	$V_{non\text{-}inv}$
4	$-V_{CC}$
5	NC
6	V_{out}
7	$+V_{CC}$
8	NC

NOTES: The chip back must be connected to $-V_{CC}$.

Connection to the "out of sequence" bond pad 4 in the packaged version is via a downbond to the substrate.

Topside Metal: Au
Backside: Si
Backside Potential: -Vcc
Mask Ref: 95
Bond Pads: .004" min

APPROVED BY:CB	**DIE SIZE: .044" x .031"**	**DATE: 1/26/01**
MFG: NATIONAL	**THICKNESS: .014"**	**P/N: CLC409**